

### Design of programmable digital down converter for WiMAX

Charanjit Singh<sup>1</sup>, Dr. Manjeet Singh Patterh<sup>1</sup> and Dr. Sanjay Sharma<sup>2</sup>

<sup>1</sup>University College of Engg., Punjabi University; <sup>2</sup>Dept. ECE, Thapar University, Patiala, Punjab, India.  
charanjit@pbi.ac.in

**Abstract:** Design of a programmable digital down converter (DDC) has been proposed, which can be used in digital receivers that meets IEEE 802.16d/e (WiMAX) standard in wireless communication system. The design is based on the idea of software radio technology and the theorem of multi-rate signal processing, It can be implemented on FPGAs and can replace traditional ASIC-based digital down converters in high channel count Software-Defined Radios.

**Keywords:** CIC Filter, digital down converter, half band filter, software defined radio, WiMAX.

#### Introduction

Software defined radio (SDR) is a wireless interface technology where multiple wireless communication standards can be implemented into a single transceiver system (Kyung-ho Hwang & Dong-ho Cho, 2000). In an SDR, most of the functions are performed by a software module implemented with a high-speed processing unit. Hence, a single hardware platform can support multiple wireless communication standards without replacing hardware components. Latest services can be incorporated just by downloading new application software. Manufacturers can provide updated wireless standards and protocol software later on through downloading at customer premises. Because SDR enables reconstructing previous systems into new systems by the direct processing of RF/IF signals with a high-speed digital signal processor and reconfigurable field-programmable gate array, it increases system interoperability and product life and minimizes developing time. In accordance with various wireless specifications and systems, transceiver systems need an open-structure that supports the simplification and alteration of their functions with flexibility. In an SDR, digital intermediate frequency (IF) processing is required because it is difficult for analog circuits to process an IF which supports all standards for various mobile telecommunication terminals. This paper proposes a solution to the problem by utilizing software defined radio technology (Reed, 2002). In the software defined radio architecture, the

reply channels are sampled at a single A/D converter and separated by Digital Down Converters (DDCs). A new architecture called channel DDC is proposed in this paper for efficient implementation of DDCs. It is an integration of conventional multi-stage FIR filters (Crochiere & Rabiner, 1983; Lim *et al.*, 1996). Fig. 1 illustrates the general structure of a DDC. A DDC converts an intermediate frequency band signal into a base band signal by using a mixer in the digital region and a low-pass filter after the analog-to-digital conversion.

#### Digital down converter architecture

Basically DDC performs the two essential software radio functions. One is frequency translation and other is channel filtering. In a basic DDC, a mixer and local oscillator perform the frequency translation. The local oscillator consists of a digital phase accumulator that advances each clock by a programmable increment equal to the tuning frequency. The phase accumulator is a register whose full-scale value represents 360 degrees of a sinusoid. A sine/cosine lookup table converts the phase angle of the accumulator to the digital voltage value of the sinusoid. The higher the increment, the faster the phase accumulator steps through the sine table. It naturally overflows at the top, preserving any residue left in the register as a phase offset for the first sample of the next cycle. As a result, the output sinusoid is directly proportional to the phase increment or frequency setting. This block is called Numerically Controlled Oscillator (NCO).

The mixer consists of two digital multipliers that accept complex sine/cosine outputs from the local oscillator and digital samples of the receiver input signal produced by an A/D converter. Multiplication in the time domain produces a sum and difference signal in the frequency domain. If the local oscillator is set to the frequency of the input signal of interest, the difference term will be that input signal translated down to 0 Hz. Since the mixer is complex, the upper and lower sidebands of the input signal will be translated to negative and positive frequencies centered at 0 Hz. The filter is a

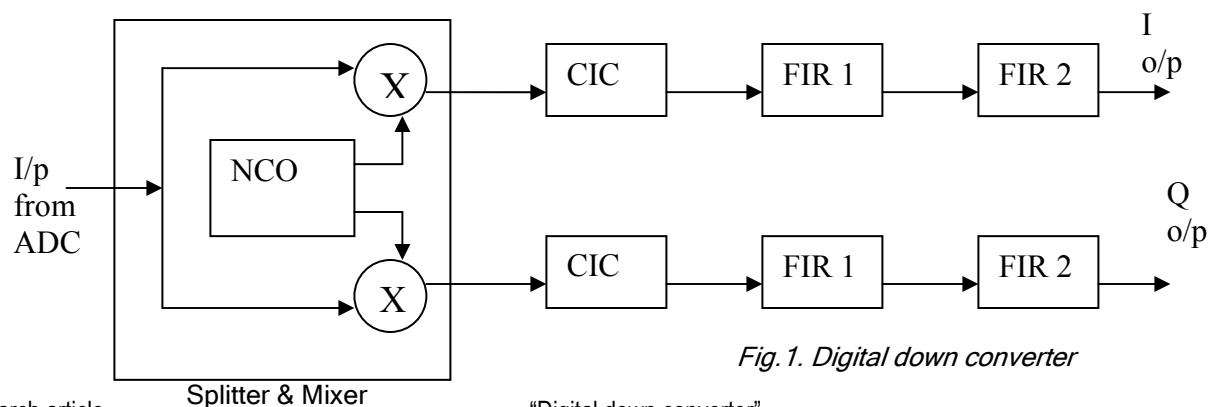


Fig. 1. Digital down converter

complex low-pass digital filter with two parallel I and Q arms whose coefficients are programmed for a pass band equal to the channel bandwidth. Because the output of the filter is band limited, the output decimation stage can drop the sampling rate accordingly. Here we used CIC filter followed by two FIR filters which can be half band filters. Although for WiMAX signal the required decimation factor will remain less than 10 so for first stage one can use either FIR filter or CIC filter but we have used CIC

in economical hardware implementation. It results in low power consumption and reduction in chip area. The magnitude response of the CIC filter is shown in Fig. 3. Proposed architecture of half band filters is shown in Fig. 4 and their frequency response are shown in Fig. 5 & 6. The overall magnitude response is shown in Fig. 7. From this it can be seen that the present efficient design is also satisfying the required spectral specifications.

**Conclusion**

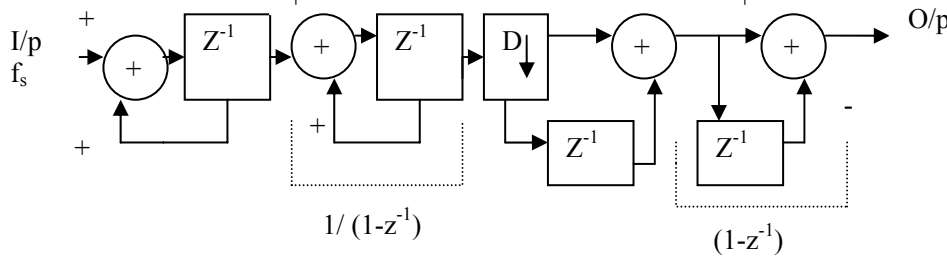
Several architectures based on the CIC filter have been considered to optimize the design. The main problem encountered is the input data flow that is not adapted to the classical CIC filter structure. We have shown that a non-recursive CIC structure followed by a half band filter can optimize the overall dissipation by making

optimum use of FPGA resources. In this paper several different filter structures suitable for digital I/Q demodulation are evaluated. A suitable structure for such a digital down converter has been considered and its implementation properties have been examined. A solution combining a CIC filter with FIR filters is found to be the most efficient solution.

**References**

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Fig. 2. Architecture of CIC Filter



filter. The CIC filter has proved to be an effective element in high decimation or interpolation systems. It is usually applied to perform the first decimation stage in analog to digital conversion and requires no multipliers. It uses limited storage resulting in economical hardware implementation. So, this choice has an impact on the design power consumption, reducing the area and the line switching associated to the computations

**CIC filter design**

The proposed CIC filter architecture is shown in Fig. 2. This kind of filter is generally applied to perform the first decimation stage in analog to digital conversion and requires no multipliers and uses limited storage resulting

Fig. 3. Magnitude response of CIC filter

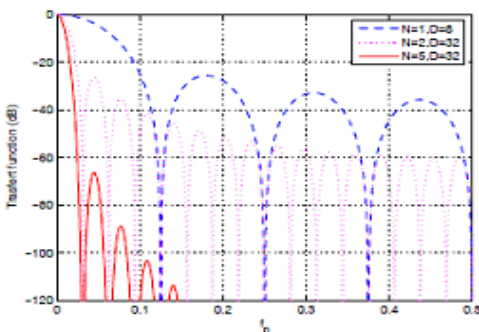


Fig. 6. Magnitude response of 2<sup>nd</sup> halfband filter

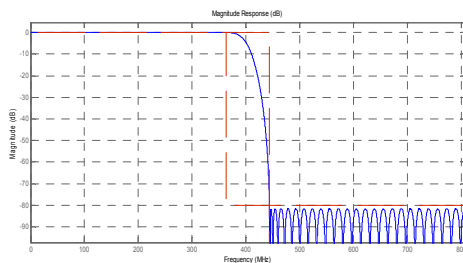


Fig. 4. Architecture of half band filter

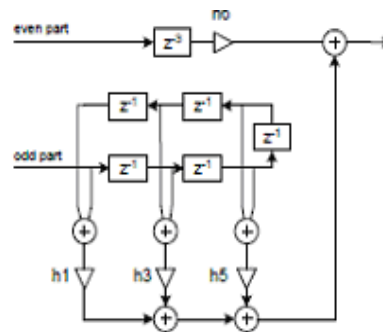


Fig. 7. Overall magnitude response of various filter sections

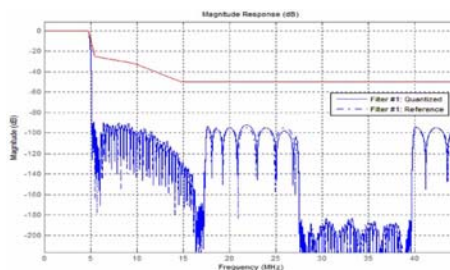
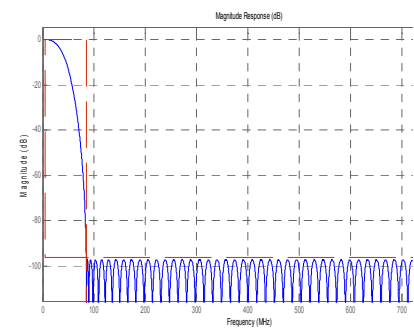


Fig. 5. Magnitude response of 1<sup>st</sup> halfband filter



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