

Proposed architect of 4-bit flash

The advantages offered by current-mode techniques are exploited in various types of ADC circuits (Chung & Yoon, 2000; Bell & Bruce, 2002; Bhat *et al.*, 2004). Recently, current-mode comparators have been used to implement analog to digital converters (Aboushady *et al.*, 2002; Bonan *et al.*, 2003; Shailesh *et al.*, 2005). In this paper, we propose architecture for 4 bit FLASH A/D converters based on a current-mode comparator. Fig.1 shows the general architecture of an N-bit Current-mode FLASH A/D Converter. It is composed of 2^N current-mode comparators. The input signal (I_{in}) is copied and distributed to all the comparators using identical PMOS current mirrors (M_{i1} , M_{i2}). A reference input current is also necessary which determines the ADC input range. The reference signal (I_{ref}) is divided to 2^N pairs of NMOS and before distributed to all the comparators gradually increases (I_1, I_2, \dots, I_{16}) using identical current mirrors ($M_{f1} \dots M_{f32}$). For 4 bit ($2^4 = 16$) we have 16 outputs. By increasing another bit ($2^5 = 32$) the number of transistors increases about two times, that is why we have used four

Fig.2. Current-Mode Comparator

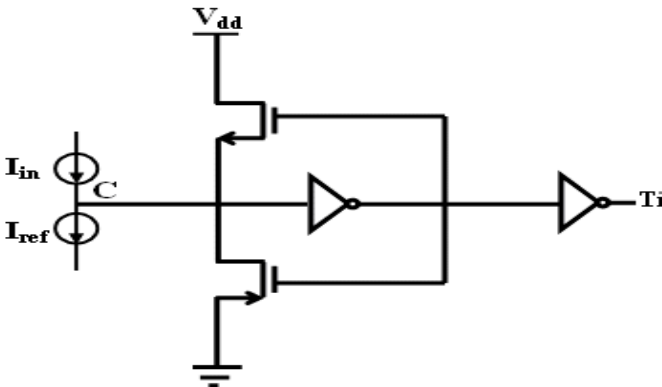


Fig.3. Thermometer to Binary Converter

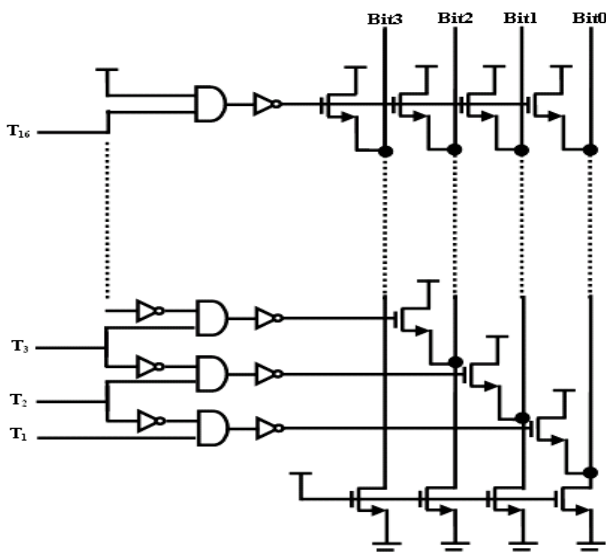
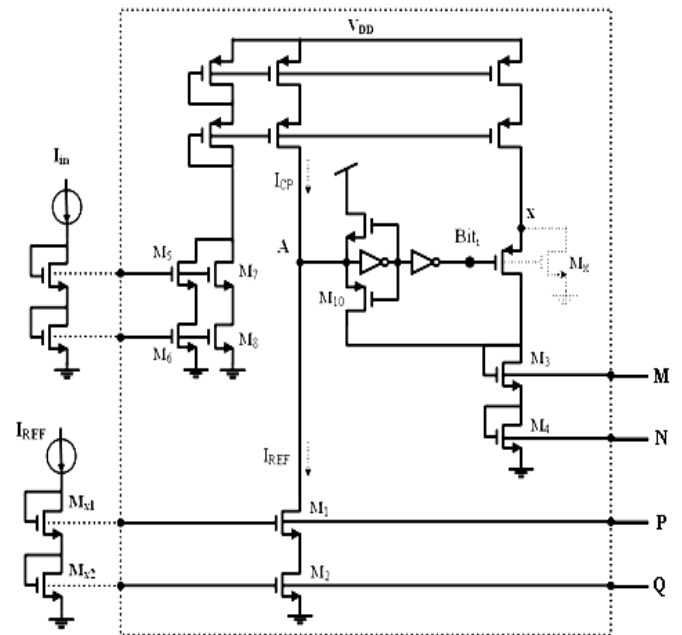


Fig. 4. The bit cell circuit of Current-Mode A/D converter and applying currents of I_{in} and I_{REF} in MSB cell



bit of this method. Fig.2 shows the current-mode comparator circuit. It is made up of NMOS and PMOS transistors and two inverters. At input of this converter (node C), I_{in} is compared to I_{ref} , If $I_{in} > I_{ref}$ the voltage of node c increases and last output of two inverters shows "1" logic, otherwise it switches to "0" logic. The output of inverter is known as thermometer and should convert to binary. Fig.3 shows a circuit that is designed to convert thermometer to binary.

Current mode successive approximation 3 bit A/D

We proposed an improved circuit based on successive approximation technique that provides a current mode A/D converter with 3bit resolution accuracy. According to the Fig. 4, two currents of I_{in} and I_{REF} are applied to the MSB cell. This structure employs continues-time algorithm data converter whose input currents of I_{in} and I_{REF} are compared together and digital outputs defined. The current of I_{REF} is mirrored in all cells and having condition of ($I_{CP} = 2I_{in} \leq 2I_{REF}$), transistors M_5 to M_8 double the current of I_{in} to provide mentioned condition: 1) If $I_{CP} > I_{REF}$, the voltage of nod A will be high and using simple current comparator, the output of nod Bit_i results logic of "1" ($Bit_i = "1"$); in this state, the residue of ($I_{CP} - I_{REF}$) enters to M_3 and M_4 from M_{10} to double in the next cell. 2) If $I_{CP} < I_{REF}$, the voltage of nod A goes low position and then the logic "0" will be obtained in output of nod Bit_i ($Bit_i = "0"$); with these, the transistor M_{11} is conducting and the current of I_{CP} is mirrored in M_3 and M_4 to double and compare in the next cell. Our proposed employed continues time algorithm data converter whose bit cells are better than previously reported (Baturone *et al.*, 2000; Gianluca *et al.*, 2002; Ivano *et al.*, 2007) which was based on that the reference current (I_{REF}) and the residue

quantity was half continuously and mirrored constant in the other cells respectively. Because of these and decreasing current in other cells, however it causes to decrease speed, encounter error and having more resolution, but increases hardware and complexity. In contrast to their works, the present circuit has capable of having low area, high speed and accuracy with more than 3bit resolution.

Non-Linearity and distortion mechanism in current mode cells

Current-mode techniques can theoretically maximize circuit performance in terms of bandwidth, slew-rate, and low voltage supply capability. Compared to their voltage-mode counter parts, current-mode circuits are more suitable for low-voltage operation because the dynamic range of the circuits is not significantly affected by a reduction in supply voltage. In addition, the compactness of these designs makes them an attractive alternative to switched capacitor when die area is restricted. Unfortunately, a major drawback of current-mode design has been the difficulty in obtaining high precision operation. This limitation was primarily due to nonlinearity introduced by the basic building block of all current-mode designs, the current copier. To achieve the best possible current matching, the device must display both a high output resistance and good device matching characteristics. To improve the device output resistance, long channel length devices must be used. Although increasing the device size reduces the device mismatches, the mismatches cannot be eliminated completely. Hence, even a sufficiently high output resistance can be obtained; the device mismatches will limit the converter accuracy as discussed in (Naris & Salania, 1990). For CMOS devices operating in the saturation region, the relative current error can be expressed as follows (Naris & Salania, 1990):

$$\frac{\Delta I}{I_{IN}} = \frac{\Delta\beta}{\beta} - \Delta V_T \left(\frac{2\beta}{I_{IN}} \right)^{1/2} \quad (1)$$

Where β , $\Delta\beta$ and, ΔV_T are the average gain constant of the mirroring devices, the difference between the gain constants of the mirroring devices, and the difference between the threshold voltages of the mirroring devices, respectively. The converters resolution will be limited by the β mismatches to 8-bit while the limitation imposed by the mismatch will depend on the signal levels and can be expressed as follows (Naris & Salania, 1990):

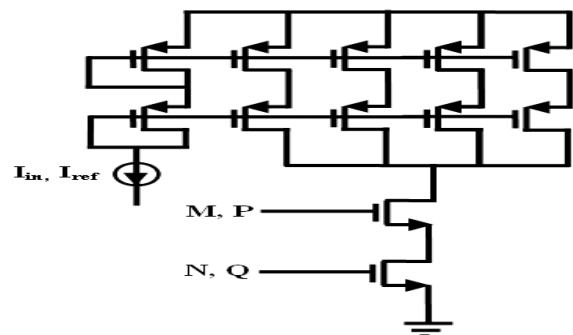
$$N = 1.44 \ln \left[\frac{V_{DD} - 3V_T}{8\Delta V_T} \right] \quad (2)$$

Therefore, if $V_{DD} = 3.3\text{-V}$, $V_T = 0.55\text{-V}$, and a 0.25% mismatch can be achieved, a maximum resolution of the 5.5-bit can be obtained. Therefore, in practice, the device mismatches will limit the converter resolution to the 8-bit range. Here because of low speed of this method we have used 3-bit resolutions.

Proposed 7 bit A/D converter

Resolution more than 4 bit in flash method makes chip die a lot and resolution more than 3 bit in successive approximation decreases speed of converter that is why here the 7-bit resolution is the best choice. Considering that the I_{ref} current is $16\ \mu\text{A}$ in 4 bit flash. Although the current of 3bit of MSB is $64\ \mu\text{A}$, it is necessary to use current divider in order to being matched. As well, I_{in} increases up to $64\ \mu\text{A}$ in entry of 4bit which must be convert to $16\ \mu\text{A}$. For providing this compatibility, it has proposed the interface circuit as shown in Fig. 5.

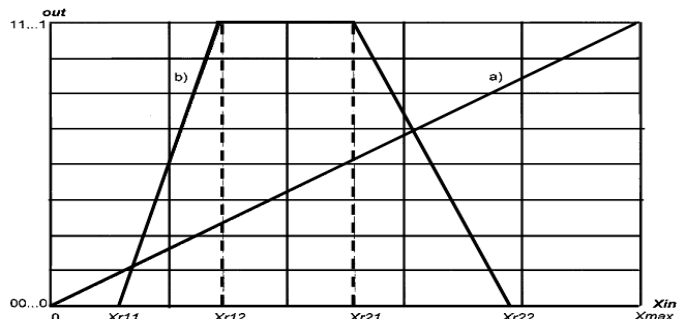
Fig.5. Interface circuit for 4bit of flash method and 3bit of successive approximation



Application of proposed A/D in fuzzification

A technique that allows the saving of a significant amount of area involves combining the A/D converter (ADC) and the subsequent fuzzification block in the same functional block (Cataldo *et al.*, 1996; Gianluca *et al.*, 2002). A design can be realized using the proposed ADC, a comparator, and some inverters and switches as it has designed in (Gianluca *et al.*, 2002). Fig.6 illustrates the transfer characteristics of a conventional ADC (curve a) and of the A/D fuzzy converter (curve b). The design parameters of the ADC are the number of bits N, and the full-scale range X_{max} , where parameter X can either be a voltage or a current. From the ADC, we can obtain an A/D fuzzy converter via nonlinear transformations. The first part (i.e., the rise edge) of the ADF transfer function is obtained by Shifting and compressing the natural A/D output in the interval $[X_{r11}, X_{r12}]$ (Chien *et al.*, 1995; Yosefi

Fig. 6. Ideal transfer characteristics: (a) conventional ADC and (b) ADC for fuzzification



et al., 2011). The second part (i.e., the falling edge) is obtained with the same technique and by complementing all the output bits (mirroring operation) in the interval $[X_{r21}, X_{r22}]$.

A general architecture which implements this idea is shown in Fig.7. It is made up of an ADC with reference input, some inverters and switches, and a comparator that selects the ADC reference input and enables output inversion by controlling the switches.

Fig. 7. Current-mode implementation of the ADC for fuzzification

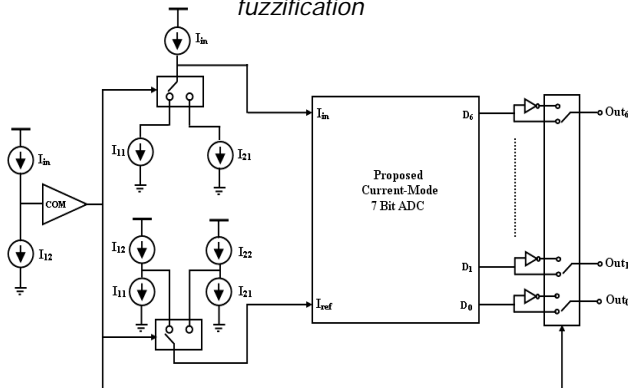


Fig. 8. Chip Die Layout

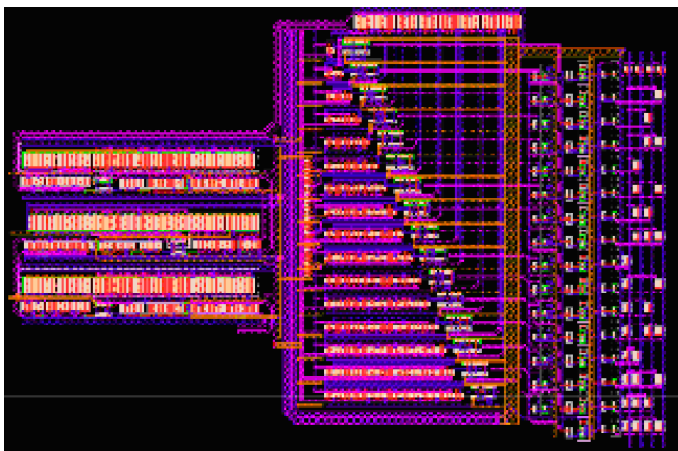
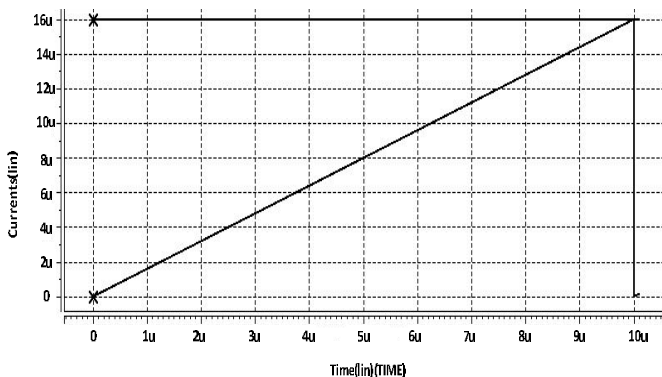


Fig.9. Input and reference currents in range 16uA, ramped and fixed shapes, respectively



When the input signal I_{in} is lower than I_{12} , the ADC reference is $I_{12}-I_{11}$ (shifting operation) and the final output is the ADC output unchanged. Otherwise, ($I_{in} > I_{12}$) the ADC reference is $I_{22}-I_{21}$, and the output is complemented. The architecture allows both the slopes of the rising/falling edges and the offset of the transcharacteristic to be set independently. Moreover, it is independent of the type of ADC. In fact, a voltage-mode or current-mode ADC can be used. Of course, all signals "X" must be replaced by their appropriate voltages or currents. Note also that the architecture requires several subtractions to be accomplished. To this end, current-mode processing other than providing low-voltage low-power circuit solutions, inherently allows the Design to be simplified. In fact, only a single node is necessary to implement a current subtraction.

Simulations

The designed 7 bit A/D converter is simulated by Hspice in 0.35μm CMOS technology. The chip Layout of the A/D conversion, extracted by the Cadence, is shown in Fig.8. The effective chip area is .02mm². As shown in Fig.9 we apply input denoted by i_{in} in ramped and constant shape. The output of the converter is illustrated

Fig.10. Simulation results of proposed 7 bit Current-Mode A/D

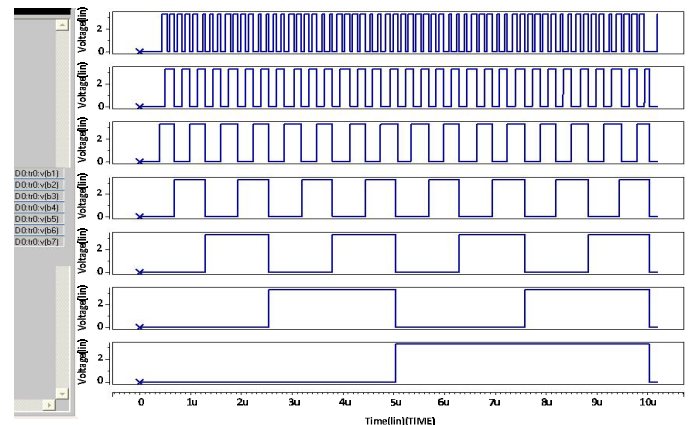


Fig.11. Trans characteristic of the designed 7-bit conventional ADC and fuzzifier ADC

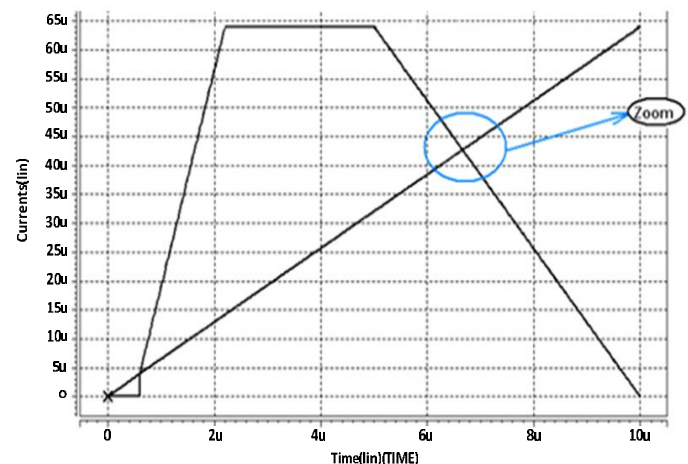
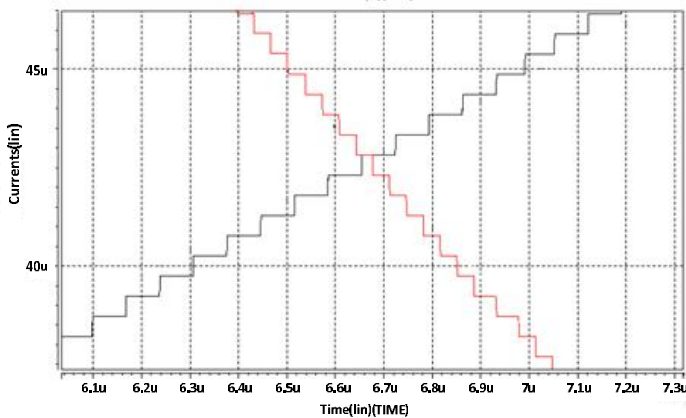


Table 1. Comparison of different reported digital membership function generators

Ref.	Technology (CMOS)	Power	Output Resolution	Speed(MFLIPS)	Membership function Shapes	Chip die(mm ²)
12	2 μm	-----	2-bit	33.33	Triangular	1.64
13	1.2 μm	-----	4-bit	30	Trapezoidal	2.34
14	0.5 μm	5.3 μW	5-bit	1.66	Triangular & Trapezoidal	0.06
15	0.35 μm	6.6 mW	4-bit	58.8	Triangular & Trapezoidal	-----
proposed	0.35 μm	5 mW	7-bits	25	Triangular & Trapezoidal	0.02

in Fig.10. It should be noted that several simulations have been performed with different input signal frequency varying from a few MHz to 25 MHz. Simulation results show that, with a power consumption of 5mW, the sampling frequency reaches 25 MHz. A 3.3-Vpower supply was used and Iref equal to 64 μA was set. Of course, the power consumption of the A/D depends on the input signal to be converted. Assuming equal probability for each input level, the average power consumption was 3.2 mW, while the maximum was 5 mW for the full-scale input.

Fig. 12. Zoomed area of fig. 11 for more clarification.



The result of applying the inputs of Fig.6 to the proposed fuzzifier is shown in Fig.11. In order to clarification, a part of the figure is zoomed in and illustrated in the Fig.12. As follows from the figure, the conventional A/D conversion and fuzzification is done simultaneously in the same functional block. This issue is a main advantage of our proposed converter.

Conclusion

A novel method for the implementation of digital triangular/trapezoidal membership function has been introduced. The 7 bit CMOS Current-Mode A/D converter makes use of parallel conversion along with successive approximation method. It performs simultaneous fuzzification and A/D converting on the same functional block. Resolution more than 4 bit in flash method, increases chip die which is vital parameter in fuzzy controller, and resolution more than 3 bit in successive approximation decreases speed of converter, that is why here the 7-bit resolution is the best choice. Therefore the proposed converter allows a significant amount of silicon area to be saved compared to fully parallel A/D It is said that the 8 bit resolution is enough for fuzzy controller (Chien *et al.*, 1995; Aminifar *et al.*, 2006).

Chien *et al.* (1995) and Ramirez *et al.*(1996) have used digital circuits to realize digital fuzzifier. In this paper we take advantages of analog circuits to implement digital fuzzifier. The proposed digital fuzzifier is capable to produce triangular, trapezoidal, S and Z shapes of fuzzification. Table 1 shows proposed fuzzifier in comparison to different digital membership function generators. The results of extracting of layout shows that it can be implemented in less than 0.02 mm² in 0.35μm CMOS standard technology. Its fully current-mode circuitry is compatible with digital processes, make it work under low power-supply voltage and high frequency. Therefore, with 5 mW power consumption in its full range, it achieves the speed of 25 MHz. The above mentioned characteristics (i.e., lower area consumption and high speed) along with high resolution (i.e., 7 bits) makes the proposed A/D well suited for using in fuzzy controllers.

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