An Efficient Technique to Reduce Average and Peak Power in Scan Based BIST

K. Thilagavathi and S. Sivanantham
School of Electronics Engineering, VIT University, Vellore - 632014, Tamil Nadu, India; thilagavathi.kmurthy@vit.ac.in, ssivanantham@vit.ac.in

Abstract

Objectives: A low-transition Test Pattern Generator (TPG) known as Bit Swapping LFSR (BS-LFSR) which generates the test vectors with low transitions. This will increase the correlation and results in one transition between the consecutive test patterns. Methods: The BS-LFSR comprises of an external XOR type LFSR along with multiplexer. The bit swapped test patterns alone is not enough to reduce the average and peak power. The Weighted Transition Metric (WTM) is calculated after shifting of test patterns into the scan cells. Based on WTM values for each test pattern, scan cells are reordered to reduce the test power. Findings: The various CUTs are chosen from ISCAS 89 standard benchmark circuits. The CUTs are synthesized using RTL Compiler tool from Cadence and the scan chain inserted Gate Level Netlist are obtained for each CUT respectively. Improvements: Experimental results show that power reduction is attained by employing the technique.

Keywords: BIST, LFSR, Scan Chain Reordering, Test Pattern Generator

1. Introduction

A wide variety of electronics equipments are being used in every aspect of life. Integrated circuits form the major component in all types of electronic systems. Along with the increasing complexity of ICs, the challenge of testing electronic systems has also grown rapidly over several years. The design for testability and Built-In-Self Test helps to decrease the overall difficulty of testing. The correlation between the test patterns is high due to very high randomness of the test patterns which will increase the switching activity at the peak. All the circuit blocks are operated simultaneously during testing. These are the main reasons for any circuit normally consumes additional power during test mode as compared to normal mode. Thus many power reduction methodologies have been established to minimize the power during testing. The focus of this paper is on minimizing the average and peak power consumption in Scan Based BISTs. Several average and peak power reduction procedures have been established to decrease the overall power that is dissipated during scan-based tests. It is always possible to use a direct method to minimize power intake by performing the test at a slower frequency compared to normal mode. Since this method is easy to implement, it significantly results in increasing test application time. Also it fails to minimize peak power as the design does not depend on clock frequency. The design of low-transition is commonly used methodology for low power tests. These algorithms generally involve modification of test vectors with a lesser transition count. The main disadvantage of this algorithm is that it aims in minimizing only the shift power consumed during the shift mode without considering the power consumed which results while the captured response is scanned out. Moreover, many of these methods result in very low fault coverage and gives rise to higher test application time.

Various low power techniques have been established to reduce the switching activity during test application in the design. One approach is to rearrange the set of test vectors in a test set for minimal power consumption. In this method, the test set is found to be of a new order, in a way that it increases the correlation between consecutive test patterns. Another technique used is a vector inhibition
technique or pseudo-random BIST to filter out vectors that are not detecting new faults. The scan chains are partitioned into multiple segments which are enabled one at a time to reduce the shift power alone with very high test application time. In addition to the above mentioned techniques a novel approach aims to bring about reduction in peak power in the capture cycle. In this method the don't care bits are assign values from a deterministic set of test vectors that brings about violation of peak power. In Scan Based BIST test patterns are generated by LFSR and shifted into the circuit through scan cells and shifted out the response through scan cells which are stored in ATE. The power dissipation in memory BIST (MBIST) is very high due to low correlation of test vectors. Adaptive test clock scheme is proposed to reduce the test application time where test clock is controlled by two ways such that, hardware control and pre-simulated stored data. The accumulator based BIST is proposed to reduce the power dissipation and increase the fault coverage with high area overhead.

This paper implements a novel technique that makes use of a low transition TPG referred as the bit swapping LFSR. The BS-LFSR is implemented using a conventional external XOR type LFSR that is combined with multiplexer. The BS-LFSR is also united along with scan chain cell reordering algorithm in order to reduce the switching activity in both the scanning cycle (shift power or average power) and the peak power involved in the test cycle.

2. Scan Based BIST

For external Scan Based testing, Automatic Test Equipment is commonly used. ATE is becoming very expensive and its cost is increasing linearly in the present scenario. Moreover the complexity in the IC’s and number of pins are increasing in the new electronic equipments. As a result Built in Self Test is one of the most important DFT methods widely used, where the internal registers are used to test the circuit. This is accomplished by mainly employing on chip test pattern generator and signature analyzer. The most conventional TPG that is used commonly being used is an external LFSR. The response/signature analyzer usually uses Multiple Input Signature Registers (MISR). When the circuit is under the test mode, the LFSR produces patterns that set the Primary Inputs (PI) in the circuit under test to values that differentiate the fault-free and also the faulty circuits and the response/signature analyzer evaluates the circuit response.

BIST can be categorized into two types based on how the test patterns are generated and applied to the circuit, namely test-per-clock and test-per-scan. The test patterns are applied to the circuit at every test clock cycle in the test-per-clock approach whereas test patterns are shifted in to the circuit only during scan mode of test-per-clock. The basic advantages of using BIST in a circuitry includes the following reasons, no expensive test equipment is required, high speed testing, lower cost of test, short test times, test can be performed throughout the operational life of the chip and dynamic properties of the circuit under test can be tested with ease.

3. BS-LFSR

This paper proposes a novel methodology that uses a low transition TPG, known as the Bit-Swapping LFSR (BS-LFSR) along with scan chain reordering. One among the major properties BS-LFSR is that it produces the mostly equal number of 1’s and 0’s at the multiplexer output, after swapping of two consecutive cells of LFSR. As a result, the probability of getting 1 or 0 becomes equal and the test vectors produced by the BS-LFSR will have low switching at the scan chain input of CUT. Also in the design of BS-LFSR, we get pseudo random values at the output of the BS-LFSR since the multiplexer output depends on mainly three different cells of the LFSR each cell containing random values as shown in Figure 2. In order to reduce the average power in scanning cycle and peak power in the scanning and test cycle, the BS-LFSR is united along with a scan chain reordering algorithm.

Two different TPG techniques are being used, an external XOR type LFSR and the bit swapping LFSR (BS-LFSR). The conventional LFSR produces patterns randomly. An n bit LFSR cycles through $2^n-1$ states (excluding all zeros). The maximum-length of an LFSR sequence is $2^n-1$ as shown in Figure 1. The BS-LFSR is based on swapping the adjacent bits of the output test vectors produced by the LFSR. The BS-LFSR is implemented using an external XOR type LFSR that is combined along with a multiplexer. The various CUT’s are chosen from ISCAS 89 benchmark circuits.
3.1 Cell Reordering Algorithm

In order to reduce both the shift and capture power, the BS-LFSR is combined with a scan cell reordering algorithm. The algorithm minimizes the transitions count between the scan cells in shift and capture mode. Shift-in and shift-out transitions are calculated by Weighted Transition Metric (WTM). For $n$ scan cells, weighted transition metric shown below $t_i$ is the test vector, where $j^{th}$ vector, $i^{th}$ bit position.

$$\text{WTM}(j) = \sum_{i=1}^{n} (t(j,i) \oplus t(j,i+1)) \ast (n-i)$$

The power due to scan in can thus be measured by adding the weighted transitions of all the test vectors in the test sequence and that due to scan out is calculated by adding weighted transitions of test response. Average power also named as shift power the average of sum of all the flip-flops transitions while shift-in and shift-out phase. The average power can be thus calculated by adding the values of scan in and scan out power and by taking the average of their sum. The peak power also named as capture power is the highest power value that is consumed at any given instant in the overall circuit design.

$$\text{AveragePower} = -(\text{WT}_{\text{scaninvector}} + \text{WT}_{\text{scanouvector}})$$

3.2 Scan Cell Reordering Procedure

Test power can be reduced by scan cell modification in the form of reordering the scan cells during test mode. This will be done following two methods namely, determining the chaining of each scan cell and finding starting and ending node of the each scan chain.

3.2.1 Determining the Order of Each Scan Cell

In scan cell ordering procedure, the first step is to calculate the weighted transition between the each scan cells is calculated. Each flip-flop in scan design is assigned a bit value corresponding to the set of scan vectors. Once the gate level Netlist is obtained, next step is to insert the scan cell into the circuit. All the flip-flops are converted into scan cell and stitched together to form scan chains. The scan vectors are applied to scan cells serially and also shifted out the test response serially in which nth flip-flop is corresponds to nth bit position and so on. The second step is to calculate the hamming distance between the each pair of flip-flops. This gives the analysis of the number of transitions (1 to 0 and 0 to 1) that is involved among these two flip-flops. From the obtained values of bit differences an undirected graph is constructed where vertices are referred to as flip-flops and bit difference is the weight of each edge between the respective pair of vertices. From this graph a minimum cost of the cycle is to be obtained. The cost refers to the sum of all the weights on the edges between flip-flops connected together in a cycle. This way the transition count occurring in the scan chain during shift operation can be minimized.

3.2.2 Identification of Scan Cell Order

The next step is to identify the scan cell order. In order to do so we have to determine the scan chain cycle that leads to reduced test power, by evaluating the $n$ possible solutions (for $n$ scan cells) during scanning in and scanning out operations described above and hence the scan cell order is selected with least weighted transition count.

3.3 Application of Scan Cell Reordering

Consider the basic $s27$ benchmark circuit as the circuit under test. The $s27$ benchmark circuit consists of 4 pri-
mary inputs, 1 primary outputs and 3 D flip-flops. Thus the scan chain size or length is equal to 3. The input of CUT is connected with the patterns generated by BS-LFSR. Simulation of Gate Level Netlist with scan chain inserted flip-flops produced the various scan in test vectors and corresponding scanned out responses. The sequences of test vectors include 000, 101,010, 111, 000 and 011. Also the corresponding output responses are 000, 101, 101, 001, 010 and 010.

3.3.1 Weighted Graph for Flip-Flops
The scan chain consists of eight flip-flops, thus the scan vectors are 8 bit long. Figure 4 shows the various test vectors and the corresponding scanned out responses involved in the s27 CUT. The arrangements shows in the Figure 3 is that the various scanned in test vector bits and the scanned output response bits associated with each of three flip-flops. Figure 4 gives the weighted undirected graph for the above scan cell arrangement. The edges of the graph connecting to flip-flops represent the total number of transitions among each flip-flop and the vertex represent each unique flip-flop.

![Figure 3](image1)

**Figure 3.** a) Scan cell arrangement; b) Test vectors.

![Figure 4](image2)

**Figure 4.** Weighted undirected graph.

3.4 Scan Chain Cycle
The scan chain cycle is obtained by stitching the reordered scan cells together in which input and output scan cells are defined in such a way that leads to low transitions. This can be done by evaluating the n possible solutions in accordance with the weighted transitions produced during scan-in and scan-out operations. The basic s27 circuit has 3 flip-flops then there are three different possible solutions of arranging the scan cells. We need to calculate the weighted transition metric for every solution which is similar to the shortest path algorithm. The selected path is the shortest path which is having minimum weighted transition among all the three paths where every node is visited exactly one at a time. One of the possible ordering of the scan cells is explained in detail and the corresponding total weighted transition is found out.

<table>
<thead>
<tr>
<th>V1</th>
<th>R1</th>
<th>V2</th>
<th>R2</th>
<th>V3</th>
<th>R3</th>
<th>V4</th>
<th>R4</th>
<th>V5</th>
<th>R5</th>
<th>V6</th>
<th>R6</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**WT for test vector V1 is (0+0+0) = 0**
**WT for test vector R1 is (0+0+0) = 0**
**WT for test vector V2 is (2+0+0) = 2**
**WT for test vector R2 is (2+0+0) = 2**
**WT for test vector V3 is (2+0+0) = 2**
**WT for test vector R3 is (2+0+0) = 2**
**WT for test vector V4 is (0+0+0) = 0**
**WT for test vector R4 is (0+1+0) = 1**
**WT for test vector V5 is (0+0+0) = 0**
WT for test vector R5 is (2+0+0) = 2
WT for test vector V6 is (2+1+0) = 3
WT for test vector R6 is (2+0+0) = 2
WT total is (0+0+2+2+2+0+1+0+2+3+2) = 16

After applying the cell reordering an all three possible scan cell arrangements, we get the total weighted transitions as 16, 21 and 18. Thus the solution having minimum amount of weighted transition is the arrangement of scan cells that gives a weighted transition of 16.

4. Experimental Results

The scan cell reordering algorithm is proposed to various ISCAS 89 benchmark circuit. The shift and capture power is calculated using equation 1 and 2. The average (shift) power and peak (capture) power is reduced up to 62% and 52% respectively. In the Table 1, the fault coverage FC, WT avg and WT pk refers to average weighted transitions and the maximum of weighted transitions per test cycle respectively. The fault coverage is calculated using BISTAD tool. Table 2 summarizes the average and peak power reduction using the proposed technique.

Table 1. Comparison of BS-LFSR and LFSR

<table>
<thead>
<tr>
<th>CUT</th>
<th>LFSR</th>
<th>BS-LFSR with Scan Chain Reordering</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>FC</td>
<td>WT avg</td>
</tr>
<tr>
<td>s641</td>
<td>94.42</td>
<td>1145.03</td>
</tr>
<tr>
<td>s838</td>
<td>86.89</td>
<td>87.60</td>
</tr>
<tr>
<td>s1196</td>
<td>91.60</td>
<td>89.78</td>
</tr>
<tr>
<td>s1238</td>
<td>88.90</td>
<td>34.28</td>
</tr>
<tr>
<td>s5378</td>
<td>94.47</td>
<td>32.98</td>
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</tbody>
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Table 2. Comparison of average and peak power

<table>
<thead>
<tr>
<th>CUT</th>
<th>% Saving of BS-LFSR</th>
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<tbody>
<tr>
<td></td>
<td>W T avg</td>
</tr>
<tr>
<td>s641</td>
<td>59</td>
</tr>
<tr>
<td>s838</td>
<td>62</td>
</tr>
<tr>
<td>s1196</td>
<td>60</td>
</tr>
<tr>
<td>s1238</td>
<td>45</td>
</tr>
<tr>
<td>s5378</td>
<td>50</td>
</tr>
</tbody>
</table>

5. Conclusion

A low transition TPG (bit swapping LFSR) that reduces the transition count at the scan chain input is implemented. The BS-LFSR reduces the transition count of the test vectors present at the scan chain. The BS-LFSR is united along with a scan cell reordering algorithm which minimizes the switching activity during both the capture and shift modes and is thus more effective than the previous techniques. To calculate the average and peak power consumed by a test sequence, the amount of weighted transitions is measured. By using the scan cell reordering algorithm, we can determine the scan cell arrangement having the minimum possible weighted transition and thus the power consumed in the circuit can be effectively reduced. The implementation of the design has no impact fault coverage and test application time. The methodology implementation can be made use of in any scan chain design techniques with more ease.

6. Future Work

The scan chain reordering is an NP complete problem. Complexity of finding the scan chain which has minimum weighted transition is very high for complex circuits. The hamiltonian cycle and greedy algorithm are applied to get low transition scan chain in the literature. In order to reduce the complexity of algorithm, conventional algorithms can be replaced with the dynamic programming. Dynamic algorithm is similar to travelling salesman algorithm which is more efficient to find the shortest path where every node is visited exactly only once.

7. References

12. Kolanchinathan VP, Saravana Kumar G. Design and implementation of the combinational circuits testing using accumulator based BIST to reduce delay, power consumption and area. Indian Journal of Science and Technology. 2016; 9(16).