An Efficient Design of Sub-threshold Logic Circuits for Ultra Low Power VLSI Applications

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Abstract

In this paper, we have provided one of the solutions for achieving ultra-low power goals. The technique used is Subthreshold region operation. This technique is useful in the applications where speed is of the secondary importance, and the low power requirement is of the prime concern. We have designed an ultra-low power sub-threshold circuits in which the voltage scaling is done below the threshold voltages. The reduction in energy consumption comes at the cost of the circuit performance. We analyzed the CMOS circuits in normal as well as sub-threshold regions and the results prove that there are orders of magnitude reduction in the power consumption.

Keywords: CMOS, Subthreshold Region, Ultra Low Power VLSI

1. Introduction

With continuous scaling of the devices, more and more number of transistors can be integrated on a single chip. Moore's law states that the transistor count on a single IC doubles after every 18 months. Thus, with higher complexity of the chips the complex computations are now possible. Along with this, portability of the devices is an overwhelming demand of the customers. Thus, weight, size and power puts some valid constraints on it. The heaviest component of the devices available today is a battery, and it has been observed that the battery technology did not evolve at the same rate as per the power requirements. Earlier, portability was associated with low handling devices like wristwatches and calculator. But nowadays, the performance of the portable devices are comparable to the high performance desktop computers. However, it has led to more power dissipation of the chips.

A decision to use any low power technique means that trade-off with some other parameters need to be done. Major criteria are delay, which will affect the performance, and the area of a chip, which directly translates to manufacturing cost factor. Some other factors to be taken care of are reliability, testability, quality, risk, etc. The conventional methods of reducing the power dissipation are governed by the golden equation of consisting of three terms: capacitance, voltage and frequency. Reducing the capacitance or the frequency is not desirable simply because it will degrade the performance of the circuits. So, the easiest way to achieve low power is to decrease the operating voltage of the CMOS circuit, as the voltage term shows the quadratic effect. However, voltage scaling leads to an increase in the sub-threshold current of the device thus leading to excessive leakage currents. Thus, one needs to think beyond the conventional methods for achieving the low power in VLSI chips.

Many other techniques and methods, like clock gating, energy recovery logic, etc. have been proposed in the past. However, in this paper, the focus lies on designing of sub-threshold circuits, one of the extreme ends of the design problem, where the supply voltage is kept lesser than the threshold voltage of the transistors. In sub-threshold region, energy consumed is very less but their speed of operation gets slowed down. Thus, such class of circuits are applicable in the areas where energy conservation is the primary constraint while as speed of operation is largely irrelevant. There is an emerging set of applications where sub-threshold logic circuits can be used. Some of them include micro-sensor networks and nodes, Radio Frequency Identification (RFID), wearable wrist...
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watch, self-powered devices, low-power digital signal processor (DSP) and MicroController Units (MCU). Some of the medical applications include pacemaker and hearing aids.

2. Sub Threshold CMOS Logic

In this section, we will model the sub-threshold logic and then its operation in the weak inversion will be explained.

- Modelling of Sub-threshold CMOS Logic

Here we will discuss the model of the MOSFET drain current in the sub-threshold region. In sub-threshold operation, transistor channel is non-inverted. The basic equation for modelling sub-threshold current is given by:

\[ I_{D(subthr)} = I_0 \exp \left( \frac{V_{GS} - V_T}{nV_{th}} \right) \]

(1)

and if the effect of \( V_{DS} \) is taken into consideration, then:

\[ I_{D(subthr)} = I_0 \exp \left( \frac{V_{GS} - V_T}{nV_{th}} \right) \left( 1 - \exp \left( -\frac{V_{DS}}{nV_{th}} \right) \right) \]

(2)

where, \( I_0 \) is the drain current when \( V_{GS} = V_T \).
\( V_T \) represents the threshold voltage.
\( V_{th} \) represents the thermal voltage.
\( N \) is the non-ideality factor.

- Operation in Sub-threshold Region

The Subthreshold logic circuits operate with a power supply \( V_{dd} \) lesser than the threshold voltage of the transistors so that the transistors are operating in the subthreshold region. We have used gpdk 180nm CMOS process kit for the simulation results, in which the threshold voltages of NMOS and PMOS are 542.623 mV and 516.801mV respectively. Drain current becomes independent of \( V_{ds} \) for all practical purposes, if \( V_{gs} > 3K_T/q \). This property has been explored so as to provide an excellent current source that spans for almost the entire rail-rail voltage range. The 3KT/q drop is usually insignificant as compared to the Vt drop in the normal strong inversion region.

Figure 1 shows the \( I_d \) versus \( V_{gs} \) curve on a logarithmic scale. The graph endorses the fact that the current does not immediately drop to zero for \( V_{gs} < V_{tn} \) but actually decays in an exponential way, represented in equations (1) and (2).

Figure 1. Gate-Source voltage v/s Drain Current in weak inversion on a logarithmic scale.

3. Design and Simulation Results

In order to estimate the power for various adiabatic logic circuits, circuits have been simulated and designed using CADENCE VIRTUOSO and SPECTRE with 180nm technology file gpdk-180 kit. Table 1 gives the details of the power dissipation under the operating conditions \( V_{dd} = 1.8 \) Volts, W and L of the NMOS and PMOS are 600nm and 180nm, respectively. The comparison of the various adiabatic logic techniques are given in Table 2. The frequency is then varied from 50 MHz to 500 MHz. The results obtained are given in figure 1.

The schematic circuit of the basic NAND gate shown in figure 4 is allowed to operate in subthreshold region. The sizing of the nmos to pmos is obtained through SPICE calculations. The PMOS to NMOS ratio is high in the subthreshold region of operation so as to get proper outputs. The capacitance of the source and drain isof major importance in effecting the outputs. By increasing the delay of the circuit in subthreshold region of operation, the power consumption is reduced. The output of the NAND gate is in figure 5.

In the same way, the schematic circuit of the basic Adiabatic 2PASCL Inverter[7-8] is shown in figure 6 and output in subthreshold operation is in figure 7.
Figure 2. Conventional CMOS Inverter in Sub-threshold region.

Figure 3. Waveforms for Conventional CMOS Inverter in Sub-threshold region.

Figure 4. Conventional NAND gate in Sub-threshold region.

Figure 5. Waveforms for Conventional NAND gate in Sub-threshold region.
4. Results and Discussion

The comparison of the various parameters like power, delay and power-delay product for CMOS inverter, CMOS NAND gate and 2PASCL inverter has been performed under strong inversion region (Table 1) as well as under sub-threshold region (Table 2).

### Table 1. Power dissipation, delay and PDP results for strong inversion region

<table>
<thead>
<tr>
<th></th>
<th>Power (in Watts)</th>
<th>Delay (in Seconds)</th>
<th>PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Inverter</td>
<td>0.429 E-6</td>
<td>0.748 E-9</td>
<td>0.320 E-15</td>
</tr>
<tr>
<td>CMOS NAND Gate</td>
<td>1.105 E-6</td>
<td>1.010 E-9</td>
<td>1.116 E-15</td>
</tr>
<tr>
<td>2PASCL Inverter</td>
<td>3.503 E-9</td>
<td>2.465 E-9</td>
<td>8.634 E-18</td>
</tr>
</tbody>
</table>

### Table 2. Power dissipation, delay and PDP results in sub-threshold region

<table>
<thead>
<tr>
<th></th>
<th>Power (in Watts)</th>
<th>Delay (in Seconds)</th>
<th>PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Inverter</td>
<td>1.034 E-9</td>
<td>4.385 E-9</td>
<td>4.534 E-18</td>
</tr>
<tr>
<td>CMOS NAND Gate</td>
<td>1.698 E-9</td>
<td>6.369 E-9</td>
<td>10.763 E-18</td>
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<tr>
<td>2PASCL Inverter</td>
<td>0.981 E-9</td>
<td>139 E-9</td>
<td>136.359 E-18</td>
</tr>
</tbody>
</table>

5. Conclusion

In this paper we have compared conventional Inverter circuit with unconventional techniques available. It has been affirmed from the calculations that the power dissipation of the adiabatic circuits are much lesser than the conventional CMOS circuits, even the input transition frequency being varied from 10 MHz to 100 MHz. Results further affirm that if PASCL technique is used then the power dissipation will be the least, but the tradeoff parameter is the speed. Hence, lesser the
power dissipation more is the delay associated with the circuit. The power delay product (PDP) parameter is the indication of how much the speed and power savings trade off has taken place in any particular technique. From the simulation results, it was further confirmed that after putting the circuits in strong inversion as well as in sub threshold region, power dissipation is tremendously improved in sub threshold region, but at the cost of higher delay.

6. References