Abstract

Background/Objectives: This paper presents timing storage circuit based on memristor emulator. The memristor emulator includes most of the characteristics of real memristor. Methods/Statistical analysis: The considerable properties that a memristor embrace are wide range of memristance, bimodal operability of pulse and continuous input signals, long period of volatility, operability with other devices. The proposed timing storage circuit stores and reproduces timing information in analog manner without performing quantization. Findings: In design of continuous-time digital FIR filter, the analog delay blocks, which are implemented using memristor, are replaced with memristor emulator based timing storage circuit. Application/Improvements: It extends its benefits of storing and reproducing the CT digital signals, wide range of memristance, and anti aliasing processing. A CT FIR filter has been designed with memristor emulator based delay block as an example

Keywords: Biomedical Signal Processing, Continuous-time Digital Signal Processing, Memristance, Memristor Emulator, Timing Storage

1. Introduction

The basic conventional DSP system samples the input and the amplitude value is quantized at the discrete sampling time for the finite-bit representation. The two processes involved are: quantization of amplitude and discretization of time. CONTINUOUS -TIME (CT) Digital Signal Processor (DSP) operates in continuous time and discrete amplitude. It convenient many applications by combining the characteristics of both Analog and Digital signals. To get motivated for CT DSP is: the major difference between the Continuous DSP system and the conventional DSP system is that, in Continuous time DSP system, the happening of event in various instants are predicted while in conventional DSP system, the small signal may change for sampling instants, so the exact timing information is lost. The CT DSP system has much less in-band distortion and higher SDR.

Our body constantly communicates the information about our health¹. Physiologic instruments are used to know that information that measures the heart rate, blood pressure, oxygen saturation levels etc.

The above measurements are analyzed and processed using biomedical signal processing to provide information useful for therapiest make conclusions. In recent days, engineers discover new methods to analyze and process these signals². The biomedical signal like Electro Cardio Graphic (ECG) signals, the signal changes fast only in short instants where at many of the times the signal vary gradually with long delays. By processing such infrequently varying signals using conventional DSP, more power is wasted on many samples that carry

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2. Memristor Emulator

The circuits used in design of FIR filter are designed at a 0.35- CMOS technology with power supply 3.3-DC V. All the blocks are customized due to the absence of clock synchronization.

2.1 Memristor Emulator-based Timing Storage Circuit and Design of Memristor Emulator with A Wide Range of Memristance Variation

The considerable properties that the proposed memristor emulator should support are a wide range of memristance, bimodal operability of pulse and continuous signal inputs and non-volatility. The proposed memristor emulator circuit includes all these features. The conventional memristor emulators have limitations particularly, the small variation in memristance and the non-floating operation are improved significantly. The memristance for an emulator is analyzed using mathematical expression. The proposed memristor emulator is a modified configuration having a small initial resistance R_s is shown in Figure 1.

At input terminal of Figure 1 the equation for voltage is

\[ V_i = R_s i_m + \alpha v_T v_C = (R_s + \alpha R_T v_C) i_m \]

where, \( v_T \) is the voltage across the resistor, \( R_T \) and \( v_C \) is the output of the analog multiplier. The sign of \( \alpha R_T v_C \) is positive and not negative.

![Figure 1. Block diagram for the memristor emulator circuit](image)

Hence, the input memristance, \( R_{in} \), is

\[ R_{in} = R_s + \alpha R_T v_C \]  

Or

...
\[ R_{in} = R_s + \frac{\alpha R_T}{C} q(t) \]  

(3)

It proves that from (3) that the input memristance is a linear function of charge \( q(t) \), thereby charge memristance dependent characteristic is achieved, although it is incremental.

Rearranging (1), we have

\[ \alpha R_T i_{in} v_C = v_{in} - R_s i_{in} \]  

(4)

To maintain the equality in (4), the feedback voltage, \( \alpha R_T i_{in} v_C \), should always be less than \( v_{in} \); namely,

\[ \alpha R_T i_{in} v_C < v_{in} \]  

(5)

Hence, \( \alpha R_T i_{in} v_C \), the output of the op-amp, is restricted not to reach the supply voltage \( V_{DD} \). In other words, the saturation of op-amp will not clip its output, \( \alpha R_T i_{in} v_C \). This is a major advantage over the existing memristor emulator since the input memristance is minimum due to the saturation of \( \alpha R_T i_{in} v_C \). From (2), minimum input resistance is obtained, \( R_{in} \), when \( v_C \) equals zero. For example, if we choose 100Ω for \( R_s \), the memristance obtained will be equal to the minimum memristance of the HP memristor.

And also, the maximum memristance is computed as the ratio between the input voltage to the input current. As the voltage across \( R_s \) is \( v_{in} - \alpha v_T v_C \), the current through \( R_s \) is

\[ i_{in} = \frac{v_{in} - \alpha v_T v_C}{R_s} \]  

(6)

\[ R_{in} \frac{v_{in}}{i_{in}} = \frac{v_{in}}{(v_{in} - \alpha v_T v_C) R_s} \]  

(7)

With (7), an infinitely large value of \( R_{in} \) can be obtained when \( \alpha v_T v_C \) approaches \( v_{in} \), as long as \( v_{in} \) is not zero.

An important result that could be pointed out is that \( \alpha v_T v_C \) does not exceed \( v_{in} \) while the input memristance, \( R_{in} \), varies from \( R_s \) to \( \infty \). In addition, as the magnitude of the input voltage, \( v_{in} \), should be less than the power voltage, \( V_{DD} \), and the feedback value \( \alpha v_T v_C \), that is obtained without the saturation of any circuit components of the proposed memristor emulator configuration. The resultant input memristance range that can be obtained using the proposed circuit configuration is theoretically from \( R_s \) to infinity.

A prompt model of memristor emulator with charge memristance dependent characteristic and wide range of memristance is designed. The section follows with timing information storage concept

3. Timing Information Storage Cell

Memristor emulator can store and reproduce information as like memristor, thereby a timing storage cell is introduced based on emulator circuit. The basic idea is described in Figure 2.

At \( t_1 \) instant, event X occurs; the memristor is connected in series with a constant current source, thereby the memristance will decrease. At \( t_2 \) instant, event Y occurs; the constant current source will be disconnected.

Figure 2. Schematic of a single timing storage cell.

The memristance value will stay constant at \( M_2 \). The difference between \( M_1 \), the initial memristance and \( M_2 \) represents the time interval between events X and Y. The constant current source is reconnected to the memristor in opposite orientation for the reproduction of timing information.

3.1 Circuit Implementation

The schematic view of a single timing storage cell using single memristor is presented in Figure 2, the memristor is replaced with memristor emulator. The CT-FIR filter is designed using memristor emulator is shown in Figure 3.

Transistors \( M_1 \) - \( M_6 \) forms a Wilson current mirror. Transistor \( M_7 \) forms switch. The J-K flip flop is configured to T flip flop by tying inputs J and K to \( V_{dd} \). This triggers the starting and ending of the reproduction phase. First
the T flip flop has to be cleared, so that the “RD_state” and “RD_start” outputs will become “0” and “1” respectively. The comparator block is responsible for detecting the instance of \( V_{\text{neg}} \) crossing \( V_{\text{ref}} \). By using delay block, the signal could be recorded and reproduced after \( \tau \) delay. The delay block is implemented using four proposed memristor emulator based timing storage circuit. For efficient area and power utilization the current mirrors and comparators are to be shared between four cells.

The “RD_start” signals are generated using a 4-bit counter. This signal starts the reproducing phase in delay blocks. Once when the delay blocks start to reproduce, the generation of square wave by counter gets stopped. The CT digital signals storage could be achieved by using memristor emulator cells which provides wide range of memristance variation \(^8\). When the ADC block produces the “Change” pulse at its output, at the same time the delay blocks are turns ON, to record the input. For the first “Change” pulse, “JK_DEL” signal is set only when the external square wave is “1” at the same time, and thereby enabling the counter. If “JK_DEL” is set and the external square wave is “0”, then the counter AND DL1 and will be ON only after the arrival of next rising edge of the square wave \(^9\). The DL1 AND gate and DL2 AND gate are included here to assure that the counter will never get enable during setup or hold time of the internal flip-flops \(^10\).

The ring counters are used to select the memristors cells in a circular order: after finishing recording or reproducing at the last memristor, from the first memristor, the operation gets continued \(^11\). The reusage of memristor cells, after each record/reproduce cycle, saves the total number of memristors cells needed. To assure the proper functioning, this condition has to be satisfied, that is, the memristor cells in the delay block should not be less than twice the number of samples that are produced in a period of \( \tau \). If this condition is not satisfied, the memristor may record an information that has not been reproduced yet \(^12\), or the memristor may reproduce a timing information from the cell that has not completed its recording.

Multiplexed addressing techniques are employed for the memristor cell selection to be more efficient \(^13\). The current mirrors used for recording and reproducing could also be reduced to one, since, for signal to be stored, simultaneous recording and reproducing of information is needed not to be done simultaneously. The “Up/Dn” bit could be simplified to tap coefficient of FIR filter such that number of multipliers required could be reduced and power and area could be effectively utilized \(^14\). The leakage power consumed by memristor emulator in timing storage circuit is hardly negligible \(^15\).

4. Observation

The simulation analysis is observed using Model sim. The output of Memristor emulator is expressed in Figures 4 and 5.

![Figure 3. Schematic of a CT FIR filter.](image)

At any instance, only one memristor cell can record and other is selected to reproduce the CT digital signal.

![Figure 4. Output of Memristor emulator.](image)
Figure 5. Output of memristor emulator.

The output for single cell timing storage cell using memristor emulator is shown in Figure 6.

Figure 6. Output for single cell timing storage cell using memristor emulator.

The output for comparator in single cell timing storage cell using memristor emulator is shown in Figure 7.

Figure 7. Output for comparator single cell timing storage cell using memristor emulator.

The output for T flip flop in single cell timing storage cell using memristor emulator is shown in Figure 8.

Figure 8. Output for T flip flop single cell timing storage cell using memristor emulator.

The output for counter in single cell timing storage cell using memristor emulator is shown in Figure 9.

Figure 9. Output for counter in single cell timing storage cell using memristor emulator.

5. Conclusion

We have presented a new timing storage circuit based on memristor emulator. The emulator memristor circuit can also store and reproduce the timing information in analog form as memristor. When incorporated in a CT DSP system, this circuit allows the infrequent varying CT digital signals to be recorded and reproduced. A continuous time FIR filter is designed with memristor based delay block, which enables the effective utilization
of power and area. It extends its benefits of wide range of memristance, long period of volatility.

6. References