Design and Simulation of Power Efficient Linear MOS Transconductor

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Abstract

Objectives: This paper proposes design of a linear and power efficient transconductance amplifier for Asynchronous Sigma Delta Modulator (ASDM). Methods/Statistical Analysis: The proposed tranconductor circuit uses two linearization techniques which have been combined for design improvement. A triode transistors configuration with cross coupled transistor pair is used to increase the linearity. Findings: The proposed transconductor is specially designed to act as a filter for ASDM. The topology attains a DC gain (A_o) of 25 dB, a Gain-Bandwidth Product (GBW) of 70 MHz, cut-off frequency of 4 MHz and a power consumption of 72.44 μW when used as an integrator. Application/Improvements: Transconductor is simulated in TSMC 0.18µm technology with an operating voltage 1.8 V. Simulation results shows that the power consumption of circuit is very less, which makes it suitable for low power signal processing applications.

Keywords: Asynchronous Sigma-Delta Modulator (ASDM), Integrator, Linearity, Power Efficient, Transconductor

1. Introduction

Integrated analog filters are the basic building block to perform different signal processing operations. One of the most common signal processing application is integrator which is considered to be very important block in Asynchronous Sigma Delta Modulator (ASDM). There are two different approaches through which analog filters can be realized: Discrete-time and continuous time implementation. Due to the sampling process, discrete-time filters are mostly used only for low frequency applications. While continuous time filters do not use sampling process so they can be used in high speed applications.

Integrated continuous time filters can be implemented using different techniques like: OPAMP-RC, MOSFET-C and G_m-C. When fabrication area is not constraint, OPAMP-RC is suitable choice as it is having good linearity. In MOSFET-C, filters resistors are replaced by MOSFET which has poor linearity compared to OPAMP-RC filters. Improvement in linearity is possible using different linearization techniques. Continuous-time filters can also be realised using G_m-C technique which has better frequency response, wider tuning range and low power consumption. G_m-C configuration uses transconductors and capacitors only and therefore such structures are simple compared to other approaches. For portable applications, power consumption is very critical parameter because battery life improves with low power circuit design.

Important consideration in G_m-C design remains in ideal characteristics of transconductance. Nonlinearity and sensitivity to parasitic capacitors are main problems related with this configuration. The linearity of transconductors can be improved through different design techniques as described in literatures. These methods include: CMOS triode transistors, crossed-coupled differential pairs, source degeneration resistor, class-AB configuration, adaptive biasing etc.
2. Circuit Configuration for Linear MOS Transconductors

The linearization can be achieved by reducing the dependence of circuit gain on input level. This can be achieved by making gain relatively independent of the transistor bias currents. In this section, two linearization techniques have been described. First one is triode MOS transistors, which is introduced in [6] and further used in [7] for ASDM design. Also used the same structure of transconductor for low power ASDM design including control on hysteresis level for comparator configuration. The second is cross coupled quad cell which is discussed in [10,11]. Proposed linear and power efficient MOS transconductor technique is presented in next section.

2.1 Transconductor using Triode MOS Transistors

The source degeneration using resistors is the simple technique to linearize input-output characteristic of MOS transconductor. There are two main disadvantages of this topology. To get wide input range, large resistor value is required and generally transconductance value is set by the degeneration resistor so tuning of the circuit is not possible in this configuration. This issue can be solved if the degeneration resistors are replaced with two parallel MOS transistors operating in the triode region. Figure 1 illustrates two parallel matched MOS transistors implemented as a resistor.

\[
I_d = \beta(V_1 - V_2) \left[ (V_g - V_{TH}) - \frac{1}{2} (V_1 - V_2) \right]
\]

\[
\text{where,} \quad \beta = \mu C_{ox} \left( \frac{W}{L} \right)
\]

Drain current for \( M_1 \) transistor is

\[
I_{d1} = \beta (V_2 - V_1) \left[ (V_{BIAS} - V_{TH}) - \frac{1}{2} (V_2 - V_1) \right]
\]

By considering perfectly matched transistors \( M_1 - M_2 \)

\[
I_{out} = I_{d1} + I_{d2} = 2\beta (V_{BIAS} - V_{TH}) (V_2 - V_1)
\]

To use \( M_1 \) and \( M_2 \) transistors as a resistor, both should remain in triode region, hence following condition should be satisfied,

\[
|V_1 - V_2| < V_{BIAS} - V_{TH}
\]

Figure 2 presents the circuit diagram of a linear CMOS transconductor introduced by [6] used it for designing integrator for Asynchronous Sigma Delta Modulator. Transistors \( M_0-M_4 \) consists of inner differential amplifier. Negative feedback has been added in the circuit through additional transistor \( M_7 \) to keep the drain source voltage across inner differential amplifier as stable as possible. Bias current \( I_{b0} \) and \( M_0-M_4 \) transistors sizes are carefully chosen for the input common mode voltage,

For small enough input voltages,

\[
V_{d3} - V_{d4} = V_{g5} - V_{g6} \approx \frac{g_{m2}}{g_{m4}} (V_{in-} - V_{in+})
\]

As \( V_{g5} = V_{g6} \) and the transconductor output current can be calculated from Eq. (5),

\[
I_{out} = I_{d1} + I_{d2} = 2\beta (V_{BIAS} - V_{TH}) V_{ad5,6}
\]

\[
= 2\beta \left[ \frac{2 I_{B1}}{\beta_p} \left( \frac{W}{L} \right) \right] \left( V_{n+} - V_{n-} \right)
\]
\[ G_m = 2\beta \frac{I_{BI}}{\beta_3} \sqrt{\frac{\beta_2}{\beta_4}} \]  

(9)

To keep \( M_5 \) and \( M_6 \) in triode region source drain voltage of \( M_5 \) transistor

\[ I_{out} = I_1 - I_2 = 2\beta V_x V_{id} \]  

(12)

where, \( \beta = \mu C_{ox} \left( \frac{W}{L} \right) \)

If aspect ratio of \( M_3 \) and \( M_4 \) transistors is kept very high, then the transconductor \( G_m \) becomes linear

\[ G_m = 2\sqrt{I\beta} \]

\( M_1 \) transistor will be turned on if \( V_{GS1} > V_{th} \) or

\[ V_1 - V_{x1} > V_{ih} \]  

(13)

To keep transconductor in its linear region \( M_1 \) transistor should be on.

When transconductor operating in linear region, \( V_{GS4} \) is confirmed to be constant. And from Figure 3(b).

\[ V_2 - V_{S1} = V_{GS4} \]  

(14)

Eq. (8) is subtracted from Eq. (9), so we get

\[ V_2 - V_1 < V_{GS4} - V_{th} \]  

When \( V_1 = V_2 \), we have

\[ \sqrt{\frac{I}{\beta}} = V_{GS1} - V_{th} = V_{GS4} - V_{th} \]

therefore the linear differential input voltage range is given by

\[ |V_{id}| < \frac{I}{\sqrt{\beta}} \]  

(15)

Figure 2. Transconductor using triode MOS transistors.

2.2 Transconductor using Cross-coupled Quad Cell

Figure 3 shows linear transconductor proposed by\(^{10}\).

Constant voltage sources \( V_x + V_{th} \) are implemented using \( M_3 \) and \( M_4 \) transistors. Width of \( M_3 \) and \( M_4 \) transistors are generally kept high compared to \( M_1 \) and \( M_2 \) transistors so biasing currents for these transistors are larger than their signal currents, which make \( V_{gs3} \) and \( V_{gs4} \) approximately constant. \( M_1 \) and \( M_2 \) transistors obey ideal square-law model,

\[ I_1 = \beta (V_x + V_{id})^2 \]  

(10)

\[ I_2 = \beta (V_x - V_{id})^2 \]  

(11)

where, \( V_{id} = V_1 - V_2 \) is the differential input voltage.

The output current obtained is given by

\[ I_{out} = I_1 - I_2 = 2\beta V_x V_{id} \]  

(12)

Figure 3(a). Schematic diagram of linear transconductor\(^{10}\) using floating voltage source.
3. Proposed Improved Linear and Power Efficient Transconductor

The core design of the transconductor is derived from\textsuperscript{(7)}; though, extra elements are added to significantly increase the linearity of the transconductor. Starting from circuit presented in Figure 1 and using cross coupled quad cell, circuit is designed which is shown in Figure 4. The sources $V_{x+}+V_{x-}$ implemented by two addition n channel transistors $M_{13}$ and $M_{14}$ biased by constant currents.

The linear differential input voltage range for inner differential stage is given by Eq. (15):

$$|V_{in}| < \frac{I_{B1}}{\beta} \quad \text{(16)}$$

The transconductor output current can be approximated by Eq. (5):

$$I_{out} = 2\beta_{n} \frac{2I_{B1}}{\beta_{s}} \left[ \frac{\mu_{p}(W/L)}{\mu_{n}(W/L)} \right]_{4} (V_{in+} - V_{in-})$$

From above equation, it can be concluded that transconductance can be tuned via $I_{B1}$. To keep $M_{5}$ and $M_{6}$ transistors in linear region:

$$|V_{id,1,2}| < \sqrt{\frac{2I_{B1}}{\beta_{s}}}$$

To investigate effect of cross coupled quad cell on overall circuit linearity, nonlinearity of source coupled differential pair should be considered. Differential circuits exhibit an “odd-symmetric” input-output characteristic\textsuperscript{(19)}. For Taylor expansion to be an odd function, all of the even-order terms must be zero:

$$\ldots + \alpha_{x}x(t) + \alpha_{x}x^{3}(t) + \alpha_{x}x^{5}(t) + \ldots$$

If load of differential pair $M_{3}$ and $M_{4}$ are matched then to calculate $V_{out1} - V_{out2}$ one can use $I_{D1}$ and $I_{D2}$ in terms of $V_{in1}$ and $V_{in2}$. If a signal $V_{m} \cos \omega t$ is applied as differential input then the amplitude of the third harmonic, $A_{HD3}$, normalized to that of the fundamental, $A_{F}$, is

$$A_{HD3} = \frac{A_{F}}{32(V_{GS} - V_{TH})^{2}}$$

For cross coupled quad cell, $V_{GS} = V_{id} + V_{x} + V_{th}$ while for simple differential amplifier $V_{GS} = V_{id}$ so compared to simple differential amplifier linearity of the cross-coupled quad cell is quite high.
4. Simulation Results

The proposed transconductor have been simulated using the standard 0.18µm TSMC CMOS technology in Cadence for 1.8 V supply voltage. Figure 5 represents the I-V characteristics of the two circuits. It is clear that modified circuit is more linear for equivalent $I_{bias}$ current as crossed coupled transistors are also added to increase the linearity of transconductor. Figure 6 represents modified circuit transconductance. As aspect ratio of cross coupled transistors are increased linearity of circuit increased for same gate length of transistors $M_1$-$M_4$. If gate length of $M_3$ and $M_4$ would be kept small compared to $M_1$ and $M_2$ transistors, then linearity range would be decreased. Figure 7 shows the Total Harmonic Distortion (THD) of the triode MOS transistors circuit and THD when cross coupled quad cell are also added to the circuit. The THD simulation result reveals noteworthy linearity improvement in modified transconductor circuit for 50MHz frequency.

![Figure 5. I-V characteristics for two linearization techniques (a) original circuit (●) (b) modified circuit with added cross coupled quad cell (●).](image)

![Figure 6. Transconductance of modified circuit for different values of W/L (a) W/L =800n/400n (○) (b) W/L= 1.6u /400n (●) (c) W/L= 400n/200n (×) (d) W/L= 800n/200n (◊).](image)

![Figure 7. Simulated THD at 50MHz for modified circuit and original circuit.](image)

The circuit diagram of integrator circuit is shown in Figure 8. The simulated dc voltage gain is 25 dB, gain-bandwidth product is 70 MHz. The magnitude and phase plots are shown in Figure 9.

![Figure 8. Application as integrator.](image)

Table 1 shows the main specifications of modified transconductance compared with some similar works. Overall transconductance of the circuit is less compared to other similar circuits, $G_m$ can be tuned via $I_{B1}$. Cut off frequency of the circuit is 4 MHz which is comparable to perform operation in HF range. Linearity improvement of the circuit is noteworthy at very high frequency range. While improvement in overall power consumption is quite significant so proposed transconductor is suitable to use in low power applications.

![Table 1](image)
5. Conclusion

The simple yet significant modifications to Lopez-Martin and Ramirez-Angulo’s transconductor circuit with improved linearity has been addressed which has been particularly designed to use with asynchronous sigma delta modulator. Proposed configuration shows significant power saving comparatively at much higher frequencies. Reduction in power consumption is possible due to reduced power supply and bias currents. The circuit provides electronic tunability by changing bias current. Instead of simple source follower, if voltage sources would be implemented using flipped voltage follower then power consumption could be further reduced.

6. References

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