A New Robust and Reliable Sub-threshold XOR Circuit with Full Output Swing

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Abstract

Objective: The aim of this work is to design a robust and reliable XOR circuit for ultra-low power operation in sub-threshold region. Method/Analysis: Comprehensive simulations have been carried out on SPICE using 16-nm predictive technology model (PTM) to accomplish our objective. Findings: A Schmitt-trigger based approach is employed to alleviate the effect of device threshold ($V_t$) fluctuation on XOR circuits. The proposed XOR circuit exhibits narrower spread in its design metrics proving its reliability in sub-45nm regime. Novelty/Improvement: This paper also analyzes various existing XOR gates in presence of process and environment (voltage and temperature) fluctuations to validate their performance. The proposed technique offers full voltage swing. Variability of the design metrics (propagation delay and power dissipation) is investigated and several XOR circuits are compared. The proposed Schmitt-trigger based XOR circuit exhibits narrower spread in its design metrics proving its reliability in sub-45nm regime.

Keywords: Full Voltage Swing, Propagation Delay, Power, Variability, XOR

1. Introduction

Process and environmental fluctuations have become the main limitation in sub-45nm regime due to aggressive scaling of CMOS technology$^{1-4}$. These fluctuations have a direct impact on system performance resulting in reduced reliability and yield loss. Therefore, these fluctuations need to be improved along with the mean values of the various design metrics.

In nano-scale regime, there are various sources of process fluctuations, which vary transistor dimensions such as gate length ($L_g$), gate width ($W_g$), $sio_2$ thickness at gate ($t_{ox}$), etc., and device threshold ($V_t$), random discrete dopant (RDD), etc. Fluctuations in gate length ($L_g$) and device threshold ($V_t$) are more dominant having variances more than 30% considering both inter-die and intra-die components$^4$.

XOR circuits find its usefulness in applications such as arithmetic operations. These arithmetic operations include design of full-adders, pseudo random sequence generator (PRSN), comparators, etc. It is also used as an important building block while designing circuits such as parity checker and parity generator circuits. Due to important roles played by XOR circuit, it is desirable to design XOR circuit, which achieves full output swing with higher reliability.

Analogies among several XOR circuits are performed in several papers but all of them are regarding the mean values of design metrics such as propagation delay ($t_p$), power dissipation (PWR).

Comprehensive simulations have been performed on SPICE using 16-nm predictive technology model to accomplish our objective$^5$.

Different configurations of XOR circuits have been reported in the literature Figure 1 to Figure 6 and there references are cited therein$^6-15$. These configurations have been used for performance comparison for this paper.

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2. Proposed Work

2.1 Output Level Improvement

As discussed earlier various XOR circuits existing in literature offer bad output levels. This problem is intolerable in sub-threshold regime when the supply voltage ($V_{DD}$) is less than $V_t$. However, XOR output with full voltage swing can be achieved by applying inverter to the output of the XNOR (XOR) circuit. But for some cases, this technique is not suitable due to extremely bad XNOR (XOR) output\(^{16}\). Moreover, the trailing inverter has shown in Figure 7 offer no improvement in the variability of the original circuit. Hence, we propose a Schmitt-trigger based XOR circuit which offers full voltage swing and considerable variability improvement.

The proposed Schmitt-trigger based XOR circuit Figure 8 uses 3-Transistor XOR circuit (Figure 1(a)) followed by a 4-Transistor Schmitt-trigger circuit. The forward body-bias applied to $P_3$ and $N_2$ results in different switching voltage or switching time which creates hysteresis to the Schmitt-trigger circuit. This hysteresis provides improved noise-margin and noise-stable application thereby, increasing the reliability of the circuit\(^ {17}\). The configuration of $P_4$ and $N_3$ is termed as dynamic-threshold MOS (DT-MOS) inverter which assures the inverter action at ultra-low-voltage of 0.4 V. The buffered output by $P_4$ and $N_3$ inverter provides rail-to-rail output swing and better driving capability.

2.2 Variability Improvement

Variability is a critical design metrics in nano-scale regime. It is defined as a statistical parameter of a circuit and is given by ratio of standard deviation ($\sigma$) of any design parameter to mean value ($\mu$) of the same design parameter. The major sources of fluctuations are the fluc-
tuation in effective gate length and device threshold. They are inter-related as
\[ V_t = V_{t0} - V_{DD} \cdot e^{-(\alpha_s \cdot L_g)} \]  
(1)

Here, \( V_{t0} \) is the long-channel \( V_t \), \( \alpha \) is the drain-induced barrier lowering coefficient. Leakage current is the driving current in the subthreshold regime given by the exponential function
\[ I \propto e^{-S \cdot V_t} \]  
(2)

where, \( S \) is the sub-threshold swing, and \( V_t \) is the threshold voltage described in (1). Additionally, sub-threshold swing \( (S) \) also depends on effective gate length \( (L_g) \). The experimental data show that they are correlated as:
\[ S = S_0 \cdot [1 + e^{(-\alpha_s \cdot L_g)}] \]  
(3)

where, \( S_0 = V_T \ln 10 \), where, \( V_T = KT/q \) is the thermal voltage and \( \alpha_s \propto (\varepsilon_{Si} t_{Si} X_{dep}/\varepsilon_{ox})^{1/2} \), where, \( \varepsilon_{Si} \) and \( \varepsilon_{ox} \) are the permittivity of Si and \( \varepsilon_{ox} \) the depletion layer thickness at gate and \( X_{dep} \) is the depletion layer thickness.

Figure 7. 3-T XOR with trailing inverter

It can be concluded from (2) and (3) that the sub-threshold current is dependent on threshold voltage \( (V_t) \), effective gate length \( (L_g) \) and supply voltage \( (V_{DD}) \), which are the critical device and environmental parameters in which fluctuations occur due to technology scaling. The fluctuations in these parameters causes fluctuation in propagation delay of a logic circuit. Based on the above equations, gate delay \( (T_d) \) is given by:\
\[ T_d = K \cdot \frac{V_{DD} - V_t}{e^{-S \cdot V_t}} \]  
(4)

Where, \( K \) is the proportionality constant (assumed). Assuming Gaussian distribution of \( L_g \) and \( V_t \), variability of delay \( (\sigma / \mu) \) of \( T_d \) can be expressed as:\
\[ \frac{\sigma_T}{T_d} = \frac{1}{T_d} \sqrt{\left[ \frac{\partial T_d}{\partial L_g} \right]^2 \cdot \sigma_{L_g}^2 + \left[ \frac{\partial T_d}{\partial V_t} \right]^2 \cdot \sigma_{V_t}^2} \]

(5)

Based on the gate delay \( (T_d) \) value given in (4), we can write:
\[ \frac{1}{T_d} \cdot \frac{\partial T_d}{\partial V_t} = e^{-S \cdot V_t} \cdot \frac{V_{DD} - V_t}{e^{-S \cdot V_t}} \cdot \frac{1}{S} \cdot \frac{\partial S}{\partial V_t} \]

(6)

It is evident from (6) that for subthreshold operation (i.e., \( V_{DD} < V_t \) ) the magnitude of \((1/T_d) \cdot (\delta T_d / \delta L_g)\) decreases with decrease in \( V_t \). Similarly,
\[ \frac{1}{T_d} \cdot \frac{\partial T_d}{\partial V_t} = e^{-S \cdot V_t} \cdot \frac{V_{DD} - V_t}{e^{-S \cdot V_t}} \cdot \frac{1}{S} \cdot \frac{\partial S}{\partial V_t} \]

Or,
\[ \frac{1}{T_d} \cdot \frac{\partial T_d}{\partial V_t} = \frac{1}{S} \]  
(7)

Figure 8. Schmitt-Trigger based XOR circuit.

As, as per (3) sub-threshold swing \( (S) \) is dependent on \( L_g \) and fluctuations in \( L_g \) are mainly due to process imperfections like line edge roughness (LER) and lithography thereby, making \( S \) a process parameter dependent. Thus, it can be inferred from (6) and (7) that delay variability depends upon a process dependent parameter \( (S) \) and an electrical parameter \( (V_t) \).
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Figure 9. (a) Input waveform A, (b) Input waveform B, (c) XOR output of previous circuit (Fig. 1(a)), (d) XOR output of proposed circuit (Fig. 8).

Table 1. Variability Analysis of Design Metrics ($t_p$, PWR) @ Supply Voltage $V_{DD} = 0.4$ V without Schmitt-Trigger Circuit

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$\sigma/\mu$ of $t_p$</th>
<th>$\sigma/\mu$ of PWR</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCMOS FA (Sum)</td>
<td>0.276</td>
<td>0.769</td>
</tr>
<tr>
<td>SCMOS FA (Carry)</td>
<td>0.275</td>
<td>0.769</td>
</tr>
<tr>
<td>SCMOS XOR</td>
<td>0.254</td>
<td>0.685</td>
</tr>
<tr>
<td>SCMOS NAND</td>
<td>0.289</td>
<td>0.694</td>
</tr>
<tr>
<td>SCMOS NOR</td>
<td>0.309</td>
<td>0.644</td>
</tr>
</tbody>
</table>

Figure 10. Propagation delay ($t_p$) variability versus supply voltage of XNOR circuits with trailing inverter.

In the proposed technique the output of the 3-T XOR circuit is passed through two inverters with dynamic body bias (see Figure 8). The body of MOSFETs $P_3$ and $N_2$ are connected to XOR (output) node resulting in either zero body bias (when XOR = 0) or forward body bias (when XOR = 1). Body bias will cause changes in $V_t$ as given by expression (8):

$$V_t = V_{t0} + \gamma \left( \sqrt{2\varphi_f - V_{th}} - \sqrt{2\varphi_f} \right)$$

where, $V_{t0}$ is the $V_t$ for $V_{BS} = 0$; $\varphi_f$ is a physical parameter with $(2\varphi_f)$ typically 0.6 V; $\gamma$ is a fabrication-process parameter.

Power consumption in sub-threshold regime is specified as

$$P_{sub} = V_{DD} \cdot I_0 \cdot e^{-\eta V_T} \left( e^{-\eta V_T} - \frac{V_{gs} - V_T}{V_T} \right)$$

where, $I_0 = \mu Cox (W/L) V_2^2 T$, $\eta$ is the subthreshold swing coefficient. It is inferred from (9), that the subthreshold current ($I_{sub}$) fluctuation causes fluctuation in subthreshold power and the fluctuations in $I_{sub}$ are caused due to fluctuation in threshold voltage. The forward body bias and DTMOS technique employed in the proposed Schmitt-trigger circuit not only decreases $V_t$ but also reduces drive current variability, thereby reducing the power variability.

Figure 11. PWR variability versus supply voltage of XNOR circuits with trailing inverter.

Table 2. Variability Analysis of Design Metrics ($t_p$, PWR) @ Supply Voltage $V_{DD} = 0.4$ V with Schmitt-Trigger Circuit

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$\sigma/\mu$ of $t_p$</th>
<th>$\sigma/\mu$ of PWR</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCMOS FA (Sum)</td>
<td>0.250</td>
<td>0.142</td>
</tr>
<tr>
<td>SCMOS FA (Carry)</td>
<td>0.254</td>
<td>0.142</td>
</tr>
<tr>
<td>SCMOS XOR</td>
<td>0.235</td>
<td>0.146</td>
</tr>
</tbody>
</table>
3. Results and Discussion

Figure 9 presents the comparison of the presented XOR circuit with its counterparts on the basis of output levels. This work also performs robustness investigation of the proposed circuit against process and environment (voltage and temperature) fluctuations. The findings of variability analysis of design parameters namely \( t_p \), PWR, are plotted in Figure 10, Figure 11 for the purpose of comparison with proposed circuit in terms of variability of \( t_p \) and PWR.

3.1 Variability Analysis of Propagation Delay

The propagation delay \( t_p \) of a gate defines how quickly it responds to a change at its inputs, i.e., it expresses the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms. The \( t_{p,LT} \) defines the response time of the gate for a low to high output transition, while \( t_{p,HT} \) refers to a high to low transition. The propagation delay \( t_p \) is defined as the average of the two \( t_p = (t_{p,LT} + t_{p,HT})/2 \). Figure 10 verify the mathematical interpretation of delay variability carried out in section 2 and proves the robustness of the proposed circuit.

3.2 Variability Analysis of Sub-threshold Power Dissipation

An outcome of average power dissipation variability is shown in Figure 11 and is evident that Schmitt-trigger based circuit offers narrower spread in power dissipation. This reduced delay variability is due to presence of DTMOS in Schmitt-Trigger which has been extensively discussed in section 2.

3.3 A circuit-level technique to design robust nano-scalesub-threshold logic circuit

Despite our implementation of Schmitt-trigger to static CMOS (SCMOS) full adder (FA), XOR, NAND and NOR circuits shown in Table 1 and Table 2, this technique is applicable to any sub-threshold CMOS logic circuits. In order to verify the proposed technique, FA, XOR, NAND and NOR circuits are simulated with SPICE employing 16-nm Predictive Technology Model (PTM). In order to capture realistic behavior, two cascaded inverters are used for all inputs and outputs of the simulation test bench with supply voltage set to \( V_{DD} = 0.4 \text{V} \). Variability of design metrics \( (t_p \text{ and PWR}) \) are estimated without and with Schmitt-trigger circuit and are presented in paper. It is apparent from the simulation results that Schmitt-trigger employed circuits offer reduced design metrics variability.

4. Conclusion

A CMOS based XOR design with improved output swing and variability of design metrics has been investigated. It also proposes Schmitt-trigger based XOR circuit. The proposed circuit presents superior performance than other discussed XOR circuits. The proposed circuit exhibits full output swing and proves its robustness and reliability against device threshold \( (V_t) \) fluctuations, which indirectly results from process and environment fluctuations. Therefore, Schmitt-trigger based XOR realization is preferred to achieve better performance against process and environment fluctuations.

5. References

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